Notice of Allowability	Application No.	Applicant(s)	
	10/039,738	MAGLIOCCO, PAUL	
	Examiner	Art Unit	
	Dieu-Minh Le	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the communication filed on 06/27/05 and interview on 09/02/05*.

2. ☒ The allowed claim(s) is/are *1-23*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☒ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☒ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)
1. ☒ Notice of References Cited (PTO-892)
2. ☒ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____.
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DIEU-MINH LE
PRIMARY EXAMINER

1. This office action is in response to the RCE filed 06/27/2005 and the interview on 09/02/2005.

2. Claims 1-23 are allowable over the prior art of record.

3. An Examiner's Amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 C.F.R. § 1.312. To ensure consideration of such an amendment, it **MUST** be submitted no later than the payment of the Issue Fee.

EXAMINER'S AMENDMENT:

IN THE CLAIMS:

Please replace all prior versions of claims in the application with the current listing claims in **SUPPLEMENTAL AMENDMENT**:

The following is an Examiner's Statement of Reasons for Allowance:

The prior arts of records do not teach nor suggest a system/method for testing a device under test [DUT], having the limitations of claims 1, 7 and 12 when viewed as a whole with the remaining limitation of the claims, in particular:

- a pattern scrambler coupled between the plurality of outputs and the plurality of T/Fs, the pattern scrambler being configured to programmably couple bits from any one or more of the plurality or outputs to any one or more of the plurality of

T/Fs, to provide a test pattern to the DUT having a programmable width of from 1 bit to a number of bits equal to the number of the plurality of outputs from the pattern memory.

4. Authorization for this Examiner's Amendment was given in a telephone interview with Ms. Jamie J. Zheng, Registration No. 51,167 on September 02, 2005.

Any comments considered necessary by applicant must be submitted no later than the payment of the Issue Fee and, to avoid processing delays, should preferably **accompany** the Issue Fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu-Minh Le whose telephone number is (571) 272-3660. The examiner can normally be reached on Monday - Thursday from 8:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)272-3645. The Tech Center 2100 phone number is (571) 272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DIEU-MINH THAI LE
PRIMARY EXAMINER
ART UNIT 2114

DML.
09/02/05

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: PAUL MAGLICCO	Examiner: LE, DIEU MINH T
Application No. 10/039,738	Art Unit: 2114
Filed: January 4, 2002	Confirmation No.: 1137
For: An Apparatus Having Pattern Scrambler For Testing A Semiconductor Device And Method For Operating Same	Date: September 2, 2005

SUPPLEMENTAL AMENDMENT

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Please amend the application as indicated on the following pages, and consider the remarks herein.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 7 of this paper.

AMENDMENT TO THE CLAIMS (II)

This listing of claims replaces all prior versions and listing of claims in the application:

1. (Currently Amended) An apparatus for testing a device under test (DUT) having a plurality of pins, the apparatus comprising:

a clock having a clock cycle;

a plurality of pin electronics channels (PEs) ~~capable of coupling~~ configured to couple to the plurality of pins on the DUT;

a plurality of timing and format circuits (T/Fs) each ~~capable of mapping~~ configured to map a signal to one of the plurality of PEs;

a pattern memory ~~capable of storing~~configured to store a number of bits for testing the DUT, the pattern memory having a plurality of *n* outputs ~~capable of outputting~~ configured to output the bits to test the DUT; and

a pattern scrambler coupled between the plurality of outputs and the plurality of T/Fs, the pattern scrambler ~~capable of being programmed to~~ being configured to programmably couple bits from any one or more of the plurality of outputs to any one or more of the plurality of T/Fs, to provide a test pattern to the DUT having a programmable width of from 1 bit to *n* bits.

2. (Currently Amended) An apparatus according to Claim 1, wherein the pattern memory has ~~*n* outputs and~~ a capacity of *m* x *n* bits, and wherein the pattern scrambler is ~~capable of being programmed to~~ configured to provide test patterns having a programmable width of from 1 bit to n bits and a programmable depth of from *n* x *m* bits to ~~a depth of *m*~~ bits.

3. (Currently Amended) An apparatus according to Claim 2, wherein the pattern scrambler is ~~capable of changing~~ configured to allow change in at least one of the width or the depth of the test patterns provided to the DUT on a cycle-by-cycle basis for each clock cycle of the test system.

4. (Currently Amended) An apparatus according to Claim 1, wherein the pattern scrambler is ~~capable of coupling~~ configured to allow bits from any one of the plurality of outputs to be coupled to any one of the plurality of PEs, and wherein the pattern scrambler is ~~capable of changing~~ configured to allow change in bits coupled to one or more of the plurality of PEs on a cycle-by-cycle basis for each clock cycle of the test system.

5. (Currently Amended) An apparatus according to Claim 1, wherein the pattern memory is ~~capable of being operated~~ configured to simultaneously provide a logic vector memory (LVM) for storing logic vectors of a number of bits and having a width and a depth, and a scan memory for storing scan vectors of a number of bits and having a width and a depth.

6. (Currently Amended) An apparatus according to Claim 5, wherein logic vectors stored in the LVM and the scan vectors stored in the scan memory comprise different widths.

7. (Currently Amended) A pattern generator for testing at least one device under test (DUT) having a plurality of pins, the pattern generator comprising:

a pattern memory ~~capable of storing~~ configured to store a number of bits for testing the DUT, the pattern memory having a plurality of *n* outputs ~~capable of outputting~~ configured to output the bits to test the DUT; and

a pattern scrambler coupled between the plurality of outputs and the plurality of pins on

the DUT, the pattern scrambler ~~capable of being programmed to~~ being configured to programmably couple bits from any one or more of the plurality of outputs to any one or more of the plurality of pins on the DUT, to provide a test pattern to the DUT having a programmable width of from 1 bit to *n* bits.

8. (Currently Amended) A pattern generator according to Claim 7, wherein the pattern memory has ~~*n* outputs and~~ a capacity of *m* x *n* bits, and wherein the pattern scrambler is ~~capable of being programmed to~~ configured to provide test patterns having a programmable width of from 1 bit to *n* bits and a programmable depth of from *n* x *m* bits to a depth of *m* bits .

9. (Currently Amended) A test system comprising a pattern generator according to Claim 8, the test system further comprising a clock having a clock cycle, and wherein the pattern scrambler is ~~capable of changing~~ configured to allow change in at least one of the width or the depth of the test patterns provided to the DUT on a cycle-by-cycle basis for each clock cycle of the test system.

10. (Currently Amended) A pattern generator according to Claim 7, wherein the pattern scrambler is ~~capable of being programmed to~~ configured to programmably couple bits from each one of the plurality of outputs to one or more of the plurality of pins on one or more DUTs.

11. (Currently Amended) A test system comprising a pattern generator according to Claim 10, the test system further comprising a clock having a clock cycle, and wherein the pattern scrambler is ~~capable of changing~~ configured to allow change in bits coupled to one or

more of the plurality of pins on one or more DUTs on a cycle-by-cycle basis for each clock cycle of the test system.

12. (Currently Amended) A pattern generator according to Claim 7, wherein the pattern scrambler is ~~capable of being operated~~ configured to simultaneously provide a logic vector memory (LVM) for delivering logic vectors of a number of bits and having a width and a depth, and a scan memory for delivering scan vectors of a number of bits and having a width and a depth.

13. A pattern generator according to Claim 12, wherein logic vectors delivered from the LVM and the scan vectors delivered from the scan memory comprise different widths.

14. A test system comprising a pattern generator according to Claim 12, the test system further comprising a clock having a clock cycle, and wherein the width of the logic vectors delivered from the LVM and the scan vectors delivered from the scan memory can be changed by the pattern scrambler on a cycle-by-cycle basis for each clock cycle of the test system.

15. (Currently Amended) A pattern generator according to Claim 7, wherein the pattern scrambler is ~~capable of being programmed to~~ configured to programmably couple a data bit of one of the plurality of outputs, output *n*, to one or more of the plurality of pins on the DUT, while strobe and I/O control bits of output *n* are coupled to one or more of the plurality of pins on the DUT, different from the one or more of the plurality of pins on the DUT to which the data bit is coupled, and wherein the I/O control bit is ~~capable of being~~ configured to be used as an expect data bit on the one or more of the plurality of pins on the DUT to which it is coupled.

16. (Currently Amended) A test system comprising a pattern generator according to Claim 7, the test system further comprising a clock having a clock cycle, and wherein the pattern scrambler is ~~capable of~~ configured to allow switching bits from any one of the plurality of outputs coupled to any one of the plurality of pins on the DUT at least twice in each clock cycle,

whereby test patterns are provided to the DUT at a rate at least twice that of the clock cycles.

17. (Currently Amended) A method for testing a device under test (DUT) using a test system including a pattern memory having a plurality of outputs equal to *n*, and a pattern scrambler coupled between the plurality of outputs and a plurality of pins on the DUT, the method comprising steps of:

storing a number of bits for testing the DUT in the pattern memory; and

programming the pattern scrambler to select, for each pin of the DUT, one or more bits from all of the plurality of outputs to be coupled to one or more of the plurality of pins on the DUT, and to provide a test pattern to the DUT having a programmable width of from 1 to *n* bits.

18. A method according to Claim 17, wherein the pattern memory has a capacity of *m* x *n* bits, and wherein the step of programming the pattern scrambler comprises the step of programming the pattern scrambler to provide test patterns having a width of from 1 bit to n bits and a depth of from *n* x *m* bits to a depth of *m* bits.

19. A method according to Claim 18, wherein the test system further comprises a clock having a clock cycle, and wherein the step of programming the pattern scrambler comprises the step of programming the pattern scrambler to change at least one of the width or

the depth of the test patterns provided to the DUT on a cycle-by-cycle basis for each clock cycle of the test system.

20. (Currently Amended) A method according to Claim 17, wherein the test system further comprises a clock having a clock cycle, and wherein the pattern scrambler is ~~capable of coupling~~ configured to allow bits from any one of the plurality of outputs be coupled to any one of the plurality of pins on the DUT, and wherein the step of programming the pattern scrambler comprises the step of programming the pattern scrambler to change bits coupled to one or more of the plurality of pins on the DUT on a cycle-by-cycle basis for each clock cycle of the test system.

21. (Currently Amended) A method according to Claim 17, wherein the pattern memory is ~~capable of being operated~~ configured to simultaneously provide a logic vector memory (LVM) and a scan memory, and wherein the step of storing a number of bits for testing the DUT in the pattern memory comprises the step of storing in the LVM logic vectors of a number of bits and having a width and a depth, and storing in the scan memory scan vectors of a number of bits and having a width and a depth.

22. A method according to Claim 21, wherein the step of storing a number of bits for testing the DUT in the pattern memory comprises the step of storing LVM vectors and the scan vectors having different widths.

23. (Currently Amended) A method according to Claim ~~11~~17, wherein the test system further comprises a clock having a clock cycle, and wherein the step of programming the pattern scrambler comprises the step of programming the pattern scrambler to switch bits from any one

of the plurality of outputs coupled to any one of the plurality of pins on the DUT at least twice in each clock cycle,

whereby test patterns are provided to the DUT at a rate at least twice that of the clock cycles.

REMARKS

Pursuant to discussions with the Examiner over the phone, claims 1-12, 15-17, 20-21, and 23 have been amended.

Prompt and favorable consideration of this Amendment and Response is respectfully requested. If the Examiner believes, for any reason, that personal communication will expedite prosecution of the application, the Examiner is invited to call the undersigned at (650) 494-8700.

Respectfully submitted,

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/Jamie J. Zheng/

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